ABSTRACT

A PLL circuit uses a multiple frequency range PLL in order to phase lock input signals having a wide range of frequencies. The PLL includes a VCO capable of operating in multiple different frequency ranges and a divider bank independently configurable to divide the output of the VCO. A frequency detector detects a frequency of the input signal and a frequency selector selects an appropriate frequency range for the PLL. The frequency selector automatically switches the PLL to a different frequency range as needed in response to a change in the input signal frequency. Frequency range hysteresis is implemented to avoid operating the PLL near a frequency range boundary.